NS6238 Datasheet

Single DP/eDP to Dual 12.8Gbps HSMT Automotive Serializer

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1. Introduction

The NS6238 serializer chip is compliant to Automotive Wired High-Speed Media Transmission (HSMT) standard. Pairing with a compatible HSMT deserializer, the NS6238 converts DisplayPort/eDP input to dual HSMT outputs for transmission of forward video and bidirectional audio and control data. Each HSMT link operates at a data rate up to 12.8Gbps in the forward direction and 100Mbps in the backward direction. The NS6238 supports 15m Coaxial cable or 8m Shielded Twisted Pair (STP) cable at 12.8Gbps. The NS6238 is AEC-Q100 Grade 2 certified with automotive temperature range of -40℃ to +105℃, and meets ISO 10605 and IEC 61000-4-2 ESD requirements.

The NS6238 supports I2C and SPI control ports, flexible GPIO with trigger mode, constant latency mode and oversample mode, tunneled UART, forward and backward audio channels, a built-in ADC, temperature sensor, and an extensive set of diagnostics.

1.1. Applications

- High-resolution Automotive Navigation System
- Central Information Display (CID)
- Digital Instrument Clusters
- Rear Seat Entertainment (RSE)
- Head Units and HMI Modules
- Rear View and Side Mirror Displays

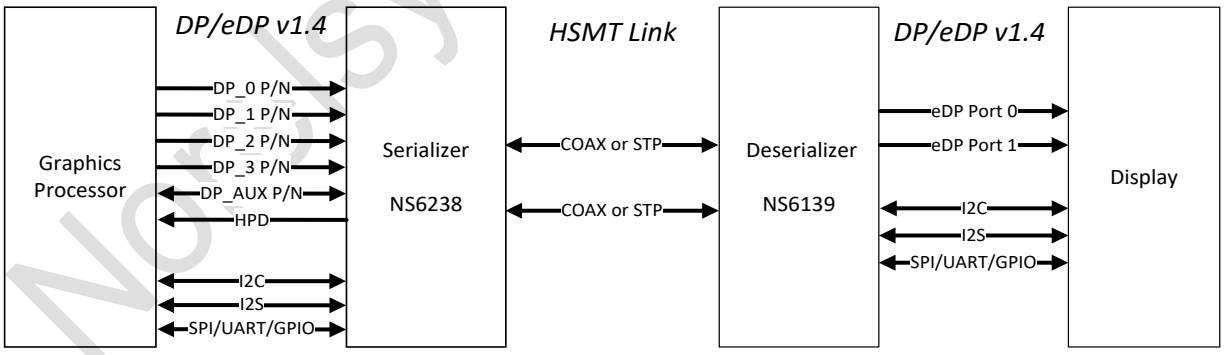


Figure 1. Application Example

1.2. Features

- Single DisplayPort input port
  - 24/30-bit RGB, and 16/20-bit YUV422
  - DP/eDP v1.4 compliant
  - 1/2/4-lane main link with up to 5.4Gbps/lane
  - Hot Plug Dectect and AUX Channel (1Mbps)
  - Supports SST or four MST streams
  - Supports 4K@60Hz resolutions
  - Supports superframe splitting to up to four video streams
  - Supports FEC
- HSMT link for system and power flexibility
  - Supports two HSMT links
  - 2.0, 3.2, 4.0, or 6.4Gbps forward-link rates per link in NRZ mode
  - 8.0 or 12.8Gbps forward-link rates per link in PAM4 mode
  - 100Mbps backward-link rate per link
- Robust communication in automotive environment
  - Backward channel adaptive equalization
  - RS-FEC for protection of forward video and bidirectional control data
  - Retransmission
  - Backward channel eye timing margin monitor for continuous link margin diagnosis
- Digital audio with I2S and TDM interface
  - Supports forward-direction 7.1 HD audio and up to 192kHz sample rate
  - Supports backward-direction 8 channels at 48kHz sample rate or 2 channels at 192kHz sample rate
- Supports bulk and tunneling modes I2C (master up to 833Kbps, slave up to 1Mbps)
- Supports SPI (master/slave up to 50Mbps), UART (TX/RX), GPIO, and interrupt for touch-screen and other use cases
- Supports data transfers I2C<->I2C, I2C<->SPI, UART<->UART, I2C->UART TX, SPI->UART TX

- CRC protection of control-channel data (I2C and SPI)
- Video watermark insertion and detection
- Video test pattern generation
- Advanced diagnostics
    - Line fault detection
    - Supply voltage monitor
- Programmble spread spectrum for EMI reduction
- 9mm x 9mm 64-pin QFN package

2. Pin Locations and Descriptions

2.1. Package Diagram with Pin Locations

Figure 2 shows the NS6238 pinout from the top of the package.

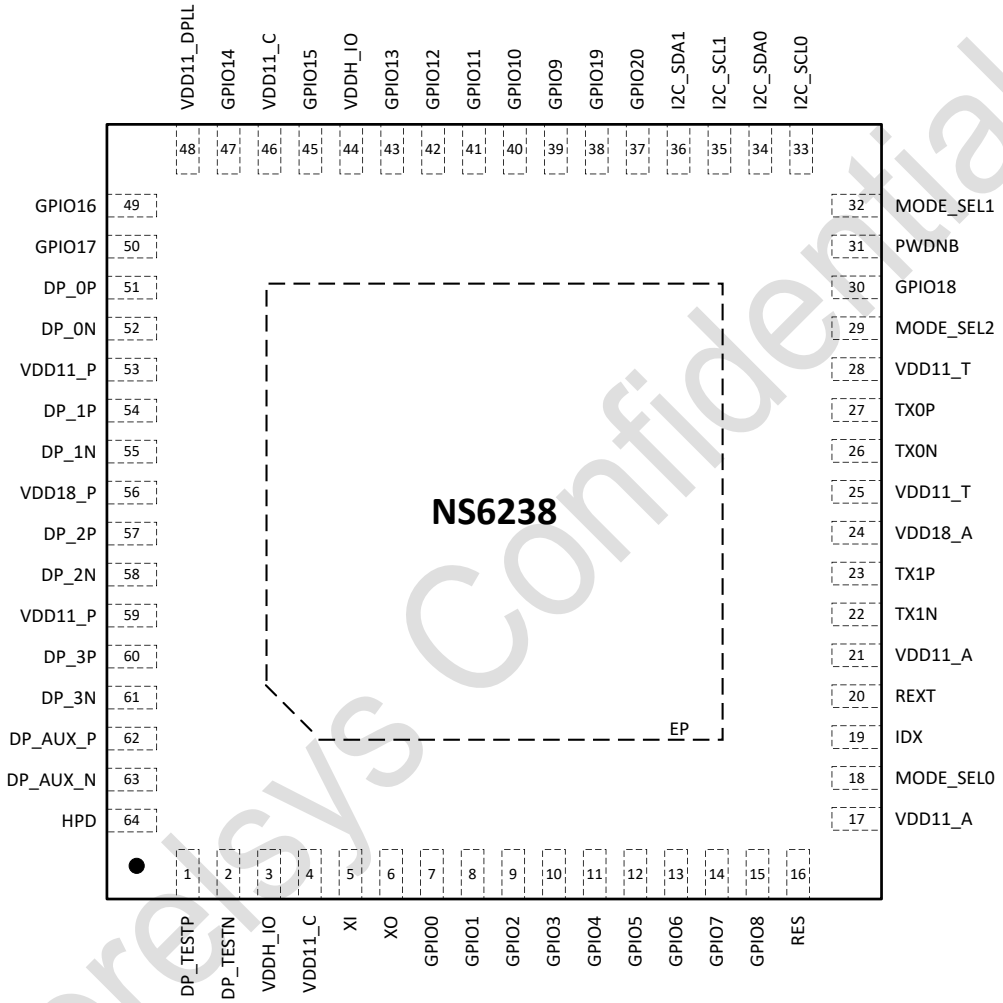


Figure 2. NS6238 Pinout

2.2. Pin Definitions

This section provides a detailed description of each signal. Table 1 is used to describe the signal type. Table 2 is used to describe the detailed pin description.

Table 1. Pin Type Description

Type	Description
I	Input
O	Output
I/O	Input/Output
HS	High speed
OD	Open drain
PH	Pull high resistor
PL	Pull low resistor
P	Power supply
G	Ground

Table 2. Pin Description

Signal Name	Pin NO.	Type	Power Supply	Description
Serial Interface				
TX0P	27	I/O, HS	VDD11_T	Positive Coax/Twisted-Pair Serial-Data Input/Output 0.
TX0N	26	I/O, HS		Negative Twisted-Pair Serial-Data Input/Output 0.
TX1P	23	I/O, HS		Positive Coax/Twisted-Pair Serial-Data Input/Output 1.
TX1N	22	I/O, HS		Negative Twisted-Pair Serial-Data Input/Output 1.
DisplayPort Interface				
DP_0P	51	I	VDD11_P	DisplayPort Main Link Lane 0 Positive Input.
DP_0N	52	I		DisplayPort Main Link Lane 0 Negative Input.
DP_1P	54	I		DisplayPort Main Link Lane 1 Positive Input.
DP_1N	55	I		DisplayPort Main Link Lane 1 Negative Input.
DP_2P	57	I		DisplayPort Main Link Lane 2 Positive Input.
DP_2N	58	I		DisplayPort Main Link Lane 2 Negative Input.
DP_3P	60	I		DisplayPort Main Link Lane 3 Positive Input.
DP_3N	61	I		DisplayPort Main Link Lane 3 Negative Input.
DP_TESTP	1	O		DisplayPort Test Port Positive Output. This pin is used for debugging purpose only.
DP_TESTN	2	O		DisplayPort Test Port Negative Output. This pin is used for debugging purpose only.

Pin Description (continued)

Signal Name	Pin NO.	Type	Power Supply	Description
DP_AUX_P	62	I/O	VDDH_IO	DisplayPort Auxiliary Channel Positive Differential Input/Output for the DisplayPort source.
DP_AUX_N	63	I/O		DisplayPort Auxiliary Channel Negative Differential Input/Output for the DisplayPort source.
HPD	64	O		Hot Plug Detect Signal Line Output for the DisplayPort source with an internal 100kΩ pulldown to ground.
Analog Signal Interface				
MODE_SEL0	18	I	VDD18_A	Mode Select 0. This pin is in VDD18_A power supply domain and the voltage to this pin is provided by a resistor divider between VDD18_A and ground.
MODE_SEL1	32	I		Mode Select 1. This pin is in VDD18_A power supply domain and the voltage to this pin is provided by a resistor divider between VDD18_A and ground.
MODE_SEL2	29	I		Mode Select 2. This pin is in VDD18_A power supply domain and the voltage to this pin is provided by a resistor divider between VDD18_A and ground.
IDX	19	I		I2C Address Select. This pin is in VDD18_A power supply domain and the voltage to this pin is provided by a resistor divider between VDD18_A and ground.
REXT	20	I		5.1kΩ ±1% external reference resistor connected between this pin and ground.
XI	5	I	VDDH_IO	Crystal Input/Oscillator Input. This pin should be connected to a 25MHz crystal or crystal oscillator.
XO	6	O		Crystal Output. If a crystal oscillator connected to XI, XO must be left open.
Multifunctional GPIO Interface				
PWDNB	31	I	VDDH_IO	Active-Low Power-Down Input with a 200kΩ Pulldown to Ground. Set PWDNB low to enter power-down mode.
GPIO0	7	I/O, PL		GPIO0 Pin with an internal 100kΩ pulldown to ground.
GPIO1	8	I/O, PL		GPIO1 Pin with an internal 100kΩ pulldown to ground.
GPIO2	9	I/O, PL		GPIO2 Pin with an internal 100kΩ pulldown to ground.
GPIO3	10	I/O, PL		GPIO3 Pin with an internal 100kΩ pulldown to ground.
GPIO4	11	I/O, PL		GPIO4 Pin with an internal 100kΩ pulldown to ground.
GPIO5	12	I/O, PL		GPIO5 Pin with an internal 100kΩ pulldown to ground.
GPIO6	13	I/O, PL		GPIO6 Pin with an internal 100kΩ pulldown to ground (enabled by default and can be disabled) or an ADC input.

Pin Description (continued)

Signal Name	Pin NO.	Type	Power Supply	Description
GPIO7	14	I/O, PL	VDDH_IO	GPIO7 Pin with an internal 100kΩ pulldown to ground.
GPIO8	15	I/O, PL		GPIO8 Pin with an internal 100kΩ pulldown to ground (enabled by default and can be disabled) or an ADC input.
GPIO9	39	I/O, PL		GPIO9 Pin with an internal 100kΩ pulldown to ground.
GPIO10	40	I/O, PL		GPIO10 Pin with an internal 100kΩ pulldown to ground.
GPIO11	41	I/O, PL		GPIO11 Pin with an internal 100kΩ pulldown to ground.
GPIO12	42	I/O, PL		GPIO12 Pin with an internal 100kΩ pulldown to ground.
GPIO13	43	I/O, PL		GPIO13 Pin with an internal 100kΩ pulldown to ground.
GPIO14	47	I/O, PL		GPIO14 Pin with an internal 100kΩ pulldown to ground.
GPIO15	45	I/O, PL		GPIO15 Pin with an internal 100kΩ pulldown to ground.
GPIO16	49	I/O, PL		GPIO16 Pin with an internal 100kΩ pulldown to ground.
GPIO17	50	I/O, PL		GPIO17 Pin with an internal 100kΩ pulldown to ground.
GPIO18	30	I/O, PL		GPIO18 Pin with an internal 100kΩ pulldown to ground.
GPIO19	38	I/O, PH		GPIO19 Pin with an internal 100kΩ pullup to V_{DDH_IO}.
GPIO20	37	I/O, PH		GPIO20 Pin with an internal 100kΩ pullup to V_{DDH_IO}.
I2C_ SCL0	33	I/O, OD		I2C 0 Clock.
I2C_SDA0	34	I/O, OD		I2C 0 Data.
I2C_SCL1	35	I/O, OD		I2C 1 Clock.
I2C_SDA1	36	I/O,OD		I2C 1 Data.
Power and Ground				
VDD11_C	4, 46	P		1.15V Core logic power supply.
VDD11_DPLL	48	P		1.15V DisplayPort PLL power supply.
VDD11_T	25, 28	P		1.15V Serial I/O power supply.
VDD11_A	17, 21	P		1.15V Analog Power supply.
VDD11_P	53, 59	P		1.15V DisplayPort power supply.
VDD18_A	24	P		1.8V Analog power supply.
VDD18_P	56	P		1.8V DisplayPort power supply.
VDDH_IO	3, 44	P		1.8V, 2.5V or 3.3V I/O power supply.
EP		G		Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.
Other Pins				
RES	16			Reserved pin.

2.3. I2C Address and Mode Select Configuration

Table 3. IDX Input Map

IDX Input Voltage (percentage of V_{DD18_A})(1)(2)			Suggested Resistor (±1% tolerance)(2)		Configuration	
Min	Typ	Max	R1(k-ohms)	R2(k-ohms)	I2C Slave 0 Address (8-bit)	I2C Slave 1 Address (8-bit)
0.0%	0.0%	7.8%	open	10	0x1C	0x1E
11.8%	14.8%	17.9%	84.5	14.7	0x24	0x26
21.9%	24.9%	27.9%	75	24.9	0x2C	0x2E
31.9%	34.9%	37.9%	64.9	34.8	0x34	0x36
41.9%	44.9%	48.1%	57.6	47	reserved	
52.1%	55.1%	58.1%	47	57.6	reserved	
62.1%	65.1%	68.1%	34.8	64.9	reserved	
72.1%	75.1%	78.1%	24.9	75	reserved	
82.1%	85.2%	88.2%	14.7	84.5	reserved	
92.2%	100.0%	100.0%	10	open	reserved	

Table 4. MODE_SEL0 Input Map

MODE_SEL0 Input Voltage (percentage of V_{DD18_A})(1)(2)			Suggested Resistor (±1% tolerance)(2)		Configuration		
Min	Typ	Max	R1(k-ohms)	R2(k-ohms)	Cable	Data Rate	Forward Link Modulation
0.0%	0.0%	7.8%	open	10	COAX/STP	6.4Gbps	NRZ
11.8%	14.8%	17.9%	84.5	14.7		4.0Gbps	NRZ
21.9%	24.9%	27.9%	75	24.9	reserved		
31.9%	34.9%	37.9%	64.9	34.8	reserved		
41.9%	44.9%	48.1%	57.6	47	COAX	12.8Gbps	PAM4
52.1%	55.1%	58.1%	47	57.6		8.0Gbps	PAM4
62.1%	65.1%	68.1%	34.8	64.9	STP	12.8Gbps	PAM4
72.1%	75.1%	78.1%	24.9	75		8.0Gbps	PAM4
82.1%	85.2%	88.2%	14.7	84.5	COAX/STP	3.2Gbps	NRZ
92.2%	100.0%	100.0%	10	open		2.0Gbps	NRZ

Table 5. MODE_SEL1 Input Map

MODE_SEL1 Input Voltage (percentage of V_{DD18_A})(1)(2)			**Suggested Resistor (±1% tolerance)(2)**		**Configuration**	
Min	Typ	Max	R1(k-ohms)	R2(k-ohms)	Auto Link	I2C Slave Speed(3)
0.0%	0.0%	7.8%	open	10	enabled	100-400kbps
11.8%	14.8%	17.9%	84.5	14.7	reserved	
21.9%	24.9%	27.9%	75	24.9	reserved	
31.9%	34.9%	37.9%	64.9	34.8	reserved	
41.9%	44.9%	48.1%	57.6	47	reserved	
52.1%	55.1%	58.1%	47	57.6	reserved	
62.1%	65.1%	68.1%	34.8	64.9	reserved	
72.1%	75.1%	78.1%	24.9	75	reserved	
82.1%	85.2%	88.2%	14.7	84.5	reserved	
92.2%	100.0%	100.0%	10	open	disabled	100-400kbps

(1) Voltage-divider resistor tolerance and V_{DD18_A} supply ripple must not cause the IDX, MODE_SEL0, or MODE_SEL1 input voltage to exceed the maximum or minimum limits.

(2) Each resistor in the voltage divider must be ≤ 100kΩ. R1 connects to V_{DD18_A}, and R2 connects to ground.

(3) The data rate of an I2C slave is up to 1Mbps, and can be programmed via the configuration register bits.

3. Package Information

3.1. 64-Pin QFN (9x9mm) Package

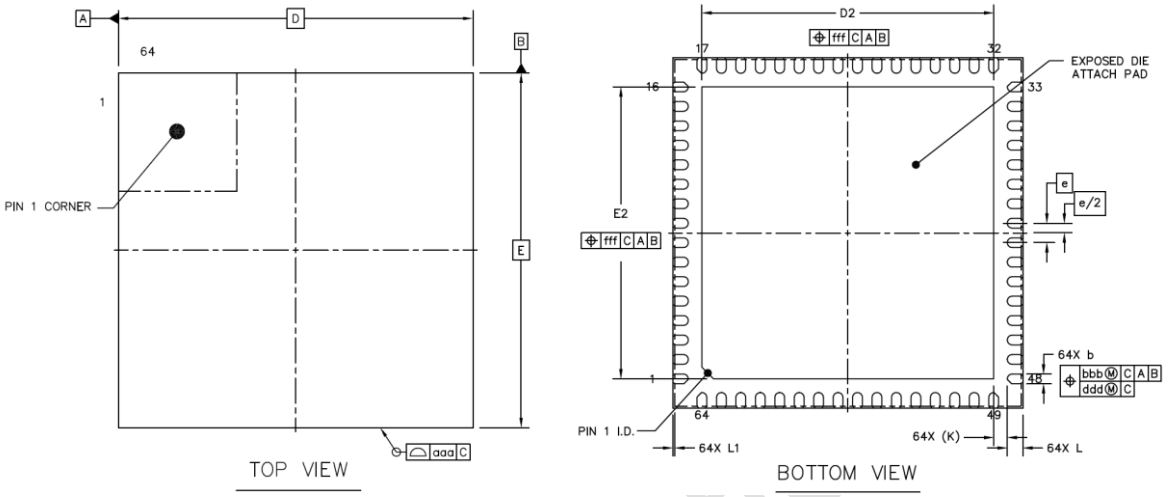
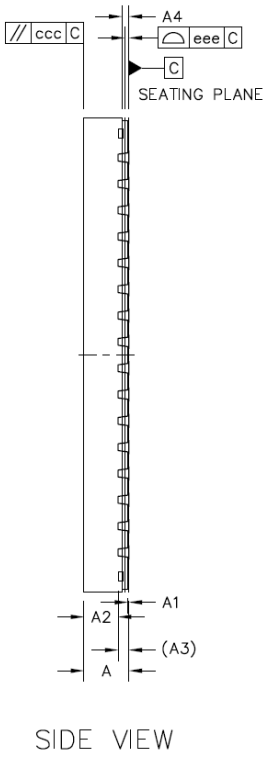


Figure 3. 64-Pin QFN Package Outline

Table 6. 64-Pin QFN Package Mechanical Data



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	7.4	7.5	7.6
	Y	E2	7.4	7.5	7.6
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	
COPLANARITY		eee		0.08	