NS6129S Datasheet

Dual 6.4Gbps HSMT to Dual OpenLDI Automotive Deserializer

Revision 0.11

Jan. 16, 2026

Norelsys

Table of Contents

List of Figures

List of Tables

1. Introduction

The NS6129S deserializer chip is compliant to Automotive Wired High-Speed Media Transmission (HSMT) standard. Pairing with a compatible HSMT serializer, the NS6129S is used for transmission of forward video and bidirectional audio and control data for automotive display applications.

The NS6129S receives the HSMT input over a single or dual HSMT links and converts the input to OpenLDI formatted output. Each HSMT link operates at a fixed data rate up to 6.4Gbps in the forward direction and 100Mbps in the backward direction. The NS6129S supports 16m Coaxial cable or 10m Shielded Twisted Pair (STP) cable. The NS6129S is AEC-Q100 Grade 2 certified with automotive temperature range of -40℃ to +105℃, and meets ISO 10605 and IEC 61000-4-2 ESD requirements.

The NS6129S is ISO 26262 ASIL-B certified and supports I2C and SPI control ports, flexible GPIO with trigger mode, constant latency mode and oversample mode, tunneled UART, forward and backward audio channels, a built-in ADC, temperature sensor, and an extensive set of diagnostics for functional safety.

Table 1. Typical Maximum Cable Length vs. Attenuation

	Dacar 302-3 50Ω Coax	RG174 50Ω Coax	100Ω STP
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.5dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, 105℃)	1.1dB/m	1.8dB/m	2.2dB/m
HSMT Forward/ Backward Data Rate	Typical Maximum Cable Length at 105℃		
3.2Gbps/100Mbps	22m	12m	12m
6.4Gbps/100Mbps	16m	10m	10m

1.1. Applications

- High-resolution Automotive Navigation System
- Central Information Display (CID)
- Digital Instrument Clusters
- Rear Seat Entertainment (RSE)
- Head Units and HMI Modules
- Rear View and Side Mirror Displays

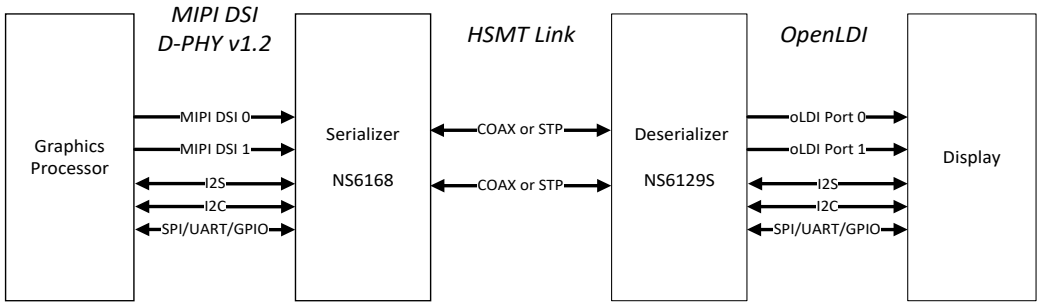


Figure 1. Application Example

1.2. Features

- Single-oLDI or dual-oLDI output ports
  - Configurable 18/24/30-bit RGB
  - Maximum pixel clock 210MHz (single-oLDI) or 420MHz (dual-oLDI)
  - Supports video aggregation
- HSMT link for system and power flexibility
  - Supports two HSMT links
  - 2.0, 3.2, 4.0, or 6.4Gbps forward-link rates in NRZ mode per link
  - 100Mbps backward-link rate per link
- Robust communication in automotive environment
  - Forward channel adaptive equalization
  - RS-FEC for protection of forward video and bidirectional control data
  - Retransmission
  - Advanced DSP continuously tracking changes in cable, connector, PCB and other channel characteristics over time and temperature
- Digital audio with I2S and TDM interface
  - Supports forward-direction 7.1 HD audio and up to 192kHz sample rate
  - Supports backward-direction 8 channels at 48kHz sample rate or 2 channels at 192kHz sample rate
- Supports bulk and tunneling modes I2C (master up to 833Kbps, slave up to 1Mbps)
- Supports SPI (master/slave up to 50Mbps), UART (TX/RX), GPIO, and interrupt for touch-screen and other use cases
- Supports data transfers I2C<->I2C, I2C<->SPI, UART<->UART, I2C->UART TX, SPI->UART TX
- Functional safety
  - AEC Q100 Grade-2 and ISO 26262 ASIL-B
  - CRC protection of control-channel data (I2C and SPI)
  - Video data error correction and retransmission
- Supports OSD (On-Screen Display)

- Supports image enhancement features
- Video watermark insertion and detection
- Video test pattern generation
- Advanced diagnostics
    - Line fault detection
    - Supply voltage monitor
- Programmble spread spectrum for EMI reduction
- 9mm x 9mm 76-pin QFN package

2. Pin Locations and Descriptions

2.1. Package Diagram with Pin Locations

Figure 2 shows the NS6129S pinout from the top of the package.

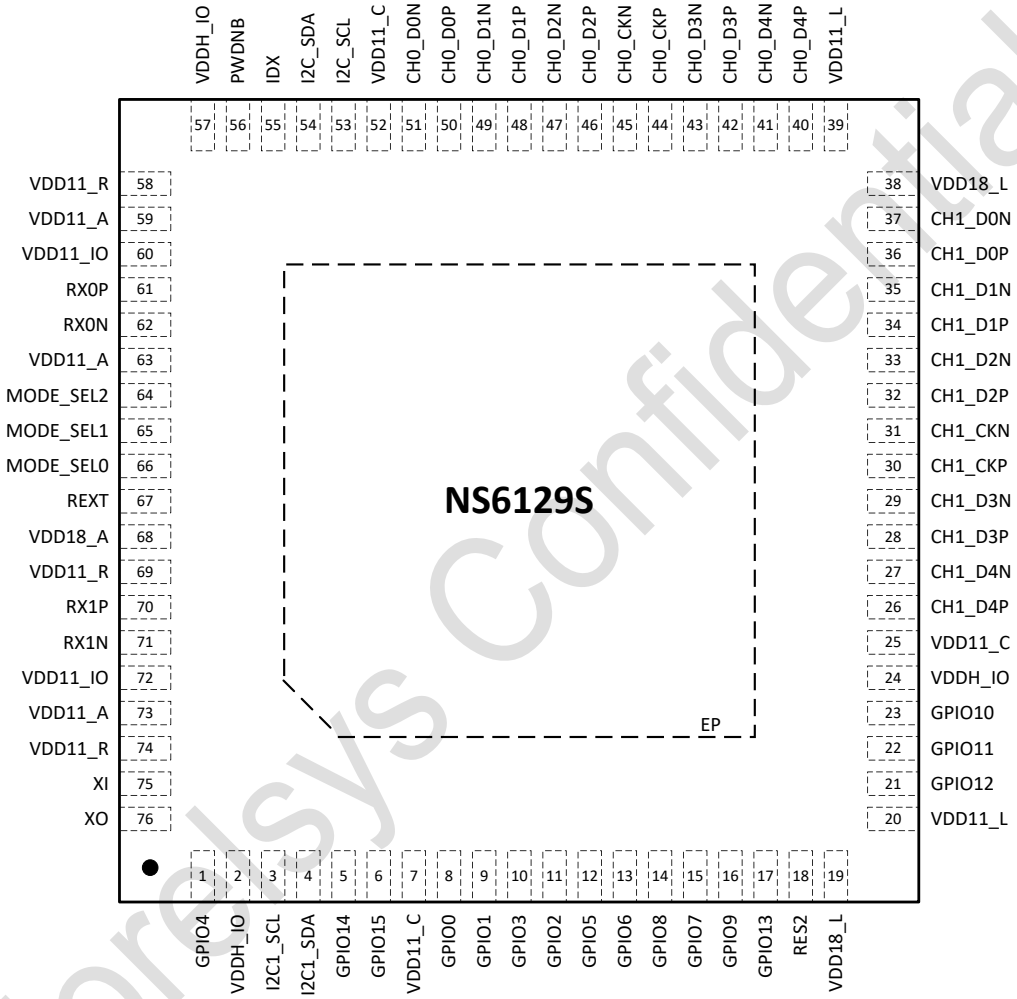


Figure 2. NS6129S Pinout

2.2. Pin Definitions

This section provides a detailed description of each signal. Table 2 is used to describe the signal type. Table 3 is used to describe the detailed pin description.

Table 2. Pin Type Description

Type	Description
I	Input
O	Output
I/O	Input/Output
HS	High speed
OD	Open drain
PH	Pull high resistor
PL	Pull low resistor
P	Power supply
G	Ground

Table 3. Pin Description

Signal Name	Pin NO.	Type	Power Supply	Description
Serial Interface				
RX0P	61	I/O, HS	VDD11_IO	Positive Coax/Twisted-Pair Serial-Data Input/Output 0.
RX0N	62	I/O, HS		Negative Twisted-Pair Serial-Data Input/Output 0.
RX1P	70	I/O, HS		Positive Coax/Twisted-Pair Serial-Data Input/Output 1.
RX1N	71	I/O, HS		Negative Twisted-Pair Serial-Data Input/Output 1.
OpenLDI Interface				
CH0_D0P	50	O	VDD18_L	oLDI Port 0 Data Lane 0 Positive Output.
CH0_D0N	51	O		oLDI Port 0 Data Lane 0 Negative Output.
CH0_D1P	48	O		oLDI Port 0 Data Lane 1 Positive Output.
CH0_D1N	49	O		oLDI Port 0 Data Lane 1 Negative Output.
CH0_D2P	46	O		oLDI Port 0 Data Lane 2 Positive Output.
CH0_D2N	47	O		oLDI Port 0 Data Lane 2 Negative Output.
CH0_CKP	44	O		oLDI Port 0 Clock Lane Positive Output.
CH0_CKN	45	O		oLDI Port 0 Clock Lane Negative Output.
CH0_D3P	42	O		oLDI Port 0 Data Lane 3 Positive Output.
CH0_D3N	43	O		oLDI Port 0 Data Lane 3 Negative Output.
CH0_D4P	40	O		oLDI Port 0 Data Lane 4 Positive Output.
CH0_D4N	41	O		oLDI Port 0 Data Lane 4 Negative Output.

Pin Description (continued)

Signal Name	Pin NO.	Type	Power Supply	Description
CH1_D0P	36	O	VDD18_L	oLDI Port 1 Data Lane 0 Positive Output.
CH1_D0N	37	O		oLDI Port 1 Data Lane 0 Negative Output.
CH1_D1P	34	O		oLDI Port 1 Data Lane 1 Positive Output.
CH1_D1N	35	O		oLDI Port 1 Data Lane 1 Negative Output.
CH1_D2P	32	O		oLDI Port 1 Data Lane 2 Positive Output.
CH1_D2N	33	O		oLDI Port 1 Data Lane 2 Negative Output.
CH1_CKP	30	O		oLDI Port 1 Clock Lane Positive Output.
CH1_CKN	31	O		oLDI Port 1 Clock Lane Negative Output.
CH1_D3P	28	O		oLDI Port 1 Data Lane 3 Positive Output.
CH1_D3N	29	O		oLDI Port 1 Data Lane 3 Negative Output.
CH1_D4P	26	O		oLDI Port 1 Data Lane 4 Positive Output.
CH1_D4N	27	O		oLDI Port 1 Data Lane 4 Negative Output.
Analog Signal Interface				
MODE_SEL0	66	I	VDD18_A	Mode Select 0. This pin is in VDD18_A power supply domain and the voltage to this pin is provided by a resistor divider between VDD18_A and ground.
MODE_SEL1	65	I		Mode Select 1. This pin is in VDD18_A power supply domain and the voltage to this pin is provided by a resistor divider between VDD18_A and ground.
MODE_SEL2	64	I		Mode Select 2. This pin is in VDD18_A power supply domain and the voltage to this pin is provided by a resistor divider between VDD18_A and ground.
IDX	55	I		I2C Address Select. This pin is in VDD18_A power supply domain and the voltage to this pin is provided by a resistor divider between VDD18_A and ground.
REXT	67	I		5.1kΩ ±1% external reference resistor connected between this pin and GND.
XI	75	I		Crystal Input/Oscillator Input. This pin should be connected to a 25MHz crystal or crystal oscillator.
XO	76	O		Crystal Output. If a crystal oscillator connected to XI, XO must be left open.
Multifunctional GPIO Interface				
PWDNB	56	I	VDDH_IO	Active-Low Power-Down Input with a 200kΩ Pulldown to Ground. Set PWDNB low to enter power-down mode.

Pin Description (continued)

Signal Name	Pin NO.	Type	Power Supply	Description
GPIO0	8	I/O, PL	VDDH_IO	GPIO0 Pin with an internal 100kΩ pulldown to ground. • If SPI Slave is enabled by setting the MODE_SEL1 input map, this pin acts as SPI_SLAVE_CK at power-up.
GPIO1	9	I/O, PL		GPIO1 Pin with an internal 100kΩ pulldown to ground.
GPIO2	11	I/O, PL		GPIO2 Pin with an internal 100kΩ pulldown to ground.
GPIO3	10	I/O, PL		GPIO3 Pin with an internal 100kΩ pulldown to ground. • If SPI Slave is enabled by setting the MODE_SEL1 input map, this pin acts as SPI_SLAVE_CSN at power-up.
GPIO4	1	I/O, PL		GPIO4 Pin with an internal 100kΩ pulldown to ground.
GPIO5	12	I/O, PL		GPIO5 Pin with an internal 100kΩ pulldown to ground. • If SPI Slave is enabled by setting the MODE_SEL1 input map, this pin acts as SPI_SLAVE_MOSI at power-up.
GPIO6	13	I/O, PL		GPIO6 Pin with an internal 100kΩ pulldown to ground (enabled by default and can be disabled) or an ADC input. • If SPI Slave is enabled by setting the MODE_SEL1 input map, this pin acts as SPI_SLAVE_MISO at power-up.
GPIO7	15	I/O, PL		GPIO7 Pin with an internal 100kΩ pulldown to ground.
GPIO8	14	I/O, PL		GPIO8 Pin with an internal 100kΩ pulldown to ground (enabled by default and can be disabled) or an ADC input.
GPIO9	16	I/O, PL		GPIO9 Pin with an internal 100kΩ pulldown to ground.
GPIO10	23	I/O, PL		GPIO10 Pin with an internal 100kΩ pulldown to ground.
GPIO11	22	I/O, PL		GPIO11 Pin with an internal 100kΩ pulldown to ground.
GPIO12	21	I/O, PL		GPIO12 Pin with an internal 100kΩ pulldown to ground.
GPIO13	17	I/O, PL		GPIO13 Pin with an internal 100kΩ pulldown to ground.
GPIO14	5	I/O, PL		GPIO14 Pin with an internal 100kΩ pulldown to ground.
GPIO15	6	I/O, PL		GPIO15 Pin with an internal 100kΩ pulldown to ground.
I2C_SDA	54	I/O, OD		I2C 0 Data.
I2C_SCL	53	I/O, OD		I2C 0 Clock.
I2C1_SDA	4	I/O, OD		I2C 1 Data.
I2C1_SCL	3	I/O, OD		I2C 1 Clock.
Power and Ground				
VDD11_A	59, 63, 73	P		1.15V Analog power supply.
VDD11_C	7, 25, 52	P		1.15V Core logic power supply.
VDD11_IO	60, 72	P		1.15V I/O power supply.
VDD11_L	20, 39	P		1.15V oLDI power supply.
VDD11_R	58, 69, 74	P		1.15V High-speed circuit power supply.

Pin Description (continued)

Signal Name	Pin NO.	Type	Power Supply	Description
VDD18_A	68	P		1.8V Analog power supply.
VDD18_L	19, 38	P		1.8V oLDI power supply.
VDDH_IO	2, 24, 57	P		1.8V, 2.5V or 3.3V I/O power supply.
EP		G		Exposed Pad. EP is internally connected to device ground. EP must be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.
Other Pins				
RES2	18			Reserved. This pin may be left as No Connect.

2.3. Multifunction Pin Assignments

NS6129S internally supports up to three I2C interfaces (either two I2C slaves + one I2C master, or two I2C masters + one I2C slave), one SPI master with up to 4 SPI_CSN output signals, one SPI slave, 20x GPIO, 2x UART TX, 2x UART RX, one I2S RX for backward direction audio supporting 8 channels at 48kHz sample rate or 2 channels at 192kHz sample rate, and two I2S TX for forward direction audio supporting 7.1 HD audio and up to 192kHz sample rate. More multifunction pin assignments are available via register configurations.

2.4. I2C Address and Mode Select Configuration

Table 4. IDX Input Map

IDX Input Voltage (percentage of V_{DD18_A})[1][2]			Suggested Resistor (±1% tolerance)[2]		Configuration	
Min	Typ	Max	R1(k-ohms)	R2(k-ohms)	I2C Slave 0 Address (8-bit)	I2C Slave 1 Address (8-bit)
0.0%	0.0%	7.8%	open	10	0x60	0x62
11.8%	14.8%	17.9%	84.5	14.7	0x68	0x6A
21.9%	24.9%	27.9%	75	24.9	0x70	0x72
31.9%	34.9%	37.9%	64.9	34.8	0x78	0x7A
41.9%	44.9%	48.1%	57.6	47	reserved	
52.1%	55.1%	58.1%	47	57.6	reserved	
62.1%	65.1%	68.1%	34.8	64.9	reserved	
72.1%	75.1%	78.1%	24.9	75	reserved	
82.1%	85.2%	88.2%	14.7	84.5	reserved	
92.2%	100.0%	100.0%	10	open	reserved	

Table 5. MODE_SEL0 Input Map

MODE_SEL0 Input Voltage (percentage of V_{DD18_A})(1)(2)			**Suggested Resistor (±1% tolerance)(2)**		**Configuration**	
Min	Typ	Max	R1(k-ohms)	R2(k-ohms)	Auto Link	Data Rate
0.0%	0.0%	7.8%	open	10	enabled	6.4Gbps NRZ
11.8%	14.8%	17.9%	84.5	14.7	reserved	
21.9%	24.9%	27.9%	75	24.9	reserved	
31.9%	34.9%	37.9%	64.9	34.8	reserved	
41.9%	44.9%	48.1%	57.6	47	enabled	2.0Gbps NRZ
52.1%	55.1%	58.1%	47	57.6	enabled	3.2Gbps NRZ
62.1%	65.1%	68.1%	34.8	64.9	enabled	4.0Gbps NRZ
72.1%	75.1%	78.1%	24.9	75	reserved	
82.1%	85.2%	88.2%	14.7	84.5	reserved	
92.2%	100.0%	100.0%	10	open	disabled	/

Table 6. MODE_SEL1 Input Map

MODE_SEL1 Input Voltage (percentage of V_{DD18_A})(1)(2)			**Suggested Resistor (±1% tolerance)(2)**		**Configuration**	
Min	Typ	Max	R1(k-ohms)	R2(k-ohms)	SPI Slave	I2C Slave Speed
0.0%	0.0%	7.8%	open	10	disabled	100-400kbps
11.8%	14.8%	17.9%	84.5	14.7	reserved	
21.9%	24.9%	27.9%	75	24.9	reserved	
31.9%	34.9%	37.9%	64.9	34.8	disabled	400-1000kbps
41.9%	44.9%	48.1%	57.6	47	reserved	
52.1%	55.1%	58.1%	47	57.6	reserved	
62.1%	65.1%	68.1%	34.8	64.9	reserved	
72.1%	75.1%	78.1%	24.9	75	reserved	
82.1%	85.2%	88.2%	14.7	84.5	enabled	400-1000kbps
92.2%	100.0%	100.0%	10	open	enabled	100-400kbps

(1) Voltage-divider resistor tolerance and V_{DD18_A} supply ripple must not cause the IDX, MODE_SEL0, or MODE_SEL1 input voltage to exceed the maximum or minimum limits.

(2) Each resistor in the voltage divider must be ≤ 100kΩ. R1 connects to V_{DD18_A}, and R2 connects to ground.

3. Package Information

3.1. 76-Pin QFN (9x9mm) Package

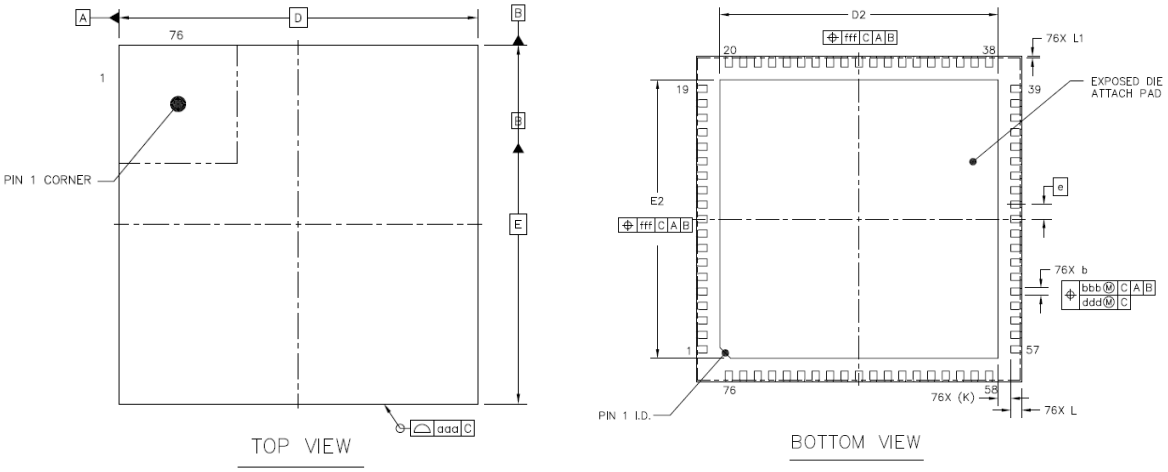
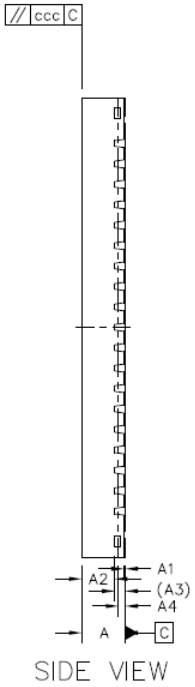


Figure 3. 76-Pin QFN Package Outline

Table 7. 76-Pin QFN Package Mechanical Data



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	7.6	7.7	7.8
	Y	E2	7.6	7.7	7.8
LEAD LENGTH		L	0.2	0.3	0.4
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	